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10/552,778	10/12/2005	Om Prakash Gangwal	NL03 0381	2059

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EXAMINER	
SHAH, TUSHAR S	

ART UNIT	PAPER NUMBER
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,778	GANGWAL, OM PRAKASH	
	Examiner	Art Unit	
	TUSHAR S. SHAH	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the application filed on October 12th, 2005.

Status of Claims

Claims 1-13 are presented for examination. Claims 1, 8, 9, 12 and 13 are in independent form. Claims 1-3, 5-10, 12 and 13 are rejected under USC 102(b). Claims 4 and 11 are rejected under USC 103(a).

Claim Objections

1. Claim 5 is objected to because of the following informalities: Claim 5 currently reads " A data processing apparatus according to Claim 5, wherein…" A claim cannot depend from itself. In order to further prosecution, claim 5 is being interpreted as if dependent from claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-10, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Nadehara US Patent No. 5,535,412 (hereinafter Nadehara).

Referring to claim 1, Nadehara discloses, a data processing apparatus, comprising a processing circuit (circular buffer controller in Fig. 6), arranged to execute a data producing process (external input register 12 for keeping a new value to be fed to the circular buffer, column 3, lines 54-56) and a data consuming process (index register 2 indicates the current object of operation, column 3, lines 36-37), the data producing process producing a stream of data (data being input into external input register 12, Fig. 6), the data consuming process consuming the stream of data concurrently with production of the stream (data is read out of data memory 4, column 4, lines 23-26);

Processing memory accessible to the data consuming process (program memory 17, Fig. 6);

A first-in first-out circular buffer unit (the circular buffer 33 is contained in data memory 4, column 4, lines 9-12) for passing data from the stream between the data producing process and the data consuming process, the circular buffer unit comprising buffer memory (data memory 4, Fig. 6), the circular buffer unit writing data-items from the stream in circular fashion into the buffer memory (the circular buffer area is an N element circular buffer, column 4, lines 10-14);

A consuming process interface of the circular buffer unit, arranged to use a grain size selection (the block length register indicates the size of the data being written into and read out of the circular buffer, column 3, lines 51-52) and an auxiliary buffer region

selection particular for the data consuming process (in order to deal with a wrap around condition a copy of the circular buffer is provided after the circular buffer area in memory, column 1, lines 60-64),

The consuming process interface being arranged to process a command for making a data grain from the stream available to the data consuming process (data from the circular buffer area is stored in data register 5 to have an arithmetic operation may be performed on it, column 5, lines 35-38), the consuming process interface being arranged to

Respond to the command by testing whether addresses of data within the grain to which access has to be gained wrap around in the buffer memory (the value of the block length register 10 is added to that of the index register 2, and the result is compared with the element number register 7 and if the value is greater than or equal to the value N, column 4, lines 52-60);

Copy, in response to detection that the addresses wrap around, the grain from the buffer memory to the auxiliary memory region, so that the wrap around is eliminated in the copied grain (in the event that an arithmetic operation is achieved beyond a circular buffer area, a copy of the circular buffer area is provided after the circular buffer area, column 1, lines 60-64); and to return an indication to the consuming process to read the grain from the buffer memory when the addresses do not wrap around inside the grain, or an indication to read from the auxiliary memory region, when the addresses wrap around (The value of the block length register is added to the index register to move the operation through the circular buffer and if the value of the resulting value of

the index is greater than the element number register, the value of the element number is subtracted from the index and the operation occurs with the values in the wrap around portion of memory otherwise the operations are carried out on the data in the range of the circular buffer area, Figs. 7 and 9).

As per claim 2, Nadehara a data processing apparatus according to Claim 1, wherein the consuming process interface is arranged to return, in response to the command, a pointer for addressing the buffer memory or the auxiliary memory region for use in address data in the grain, dependent on whether the addresses of the data in the grain in the buffer memory wrap around (the value of the block length register is added to the index register to move the operation through the circular buffer and if the value of the resulting value of the index is greater than the element number register, the value of the element number is subtracted from the index and the operation occurs with the values in the wrap around portion of memory otherwise the operations are carried out on the data in the range of the circular buffer area, Figs. 7 and 9).

As per claim 3, Nadehara discloses, the consuming process is arranged to select an address of the auxiliary memory and the grain size as part of the command (Step 106, Fig. 7).

As per claim 5, Nadehara discloses, the data producing process is arranged to use variable grain sizes for sending data (the block length register specifies the size of

data to be processed at a time and it is seen as inherent that it may change, column 3, lines 51-52).

As per claim 6, Nadehara discloses, the first grain size and a size of the circular buffer unit are selected so that addresses of the data in the circular buffer unit always wrap around between successive grains of the first grain size (It is identified by Nadehara that this is the standard operation of prior art systems, column 1, lines 53-57 and Fig 5).

As per claim 7, Nadehara discloses, containing a further processing memory (circular buffer controller in Fig. 6) accessible to a data producing process (external input register 12 for keeping a new value to be fed to the circular buffer, column 3, lines 54-56) for producing the data stream;

A producing process interface (External input register, Fig. 6) of the circular buffer unit, arranged to receive a further auxiliary memory region selection for the data producing process (in order to deal with a wrap around condition a copy of the circular buffer is provided after the circular buffer area in memory, column 1, lines 60-64), the producing process interface being arranged to process a further command for outputting an output data grain from the stream (data from the circular buffer area is stored in data register 5 to have an arithmetic operation may be performed on it, column 5, lines 35-38), the producing process interface being arranged to respond to the further command

by testing whether addresses of data within the output grain to will wrap around in the buffer memory step 123, Fig. 8);

To return an indication to the producing process to write the grain to the buffer memory when the addresses do not wrap around inside the grain, or an indication to write to the auxiliary memory region, when the addresses wrap around (if the value of the input index register is greater than the value of the block length register, the value of the element number register is added to the write address to generate the replica addresses past the circular buffer area, Fig. 8);

Copy, in response to detection that the addresses wrap around, the grain from auxiliary memory region to the buffer memory so that the wrap around is created in the copied grain (the values from the external input register are written into the replica addresses in a wrap around, Fig. 8).

Referring to claim 8, Nadehara discloses, a data processing apparatus, comprising: a processing circuit (circular buffer controller in Fig. 6), arranged to execute a data producing process (external input register 12 for keeping a new value to be fed to the circular buffer, column 3, lines 54-56) and a data consuming process (index register 2 indicates the current object of operation, column 3, lines 36-37), the data producing process producing a stream of data (data being input into external input register 12, Fig. 6), the data consuming process consuming the stream of data concurrently with production of the stream (data is read out of data memory 4, column 4, lines 23-26);

Processing memory accessible to the data producing process (program memory 17, Fig. 6);

A first-in first-out circular buffer unit (the circular buffer 33 is contained in data memory 4, column 4, lines 9-12) for passing data from the stream between the data producing process and the data consuming process, the circular buffer unit comprising buffer memory (data memory 4, Fig. 6), the circular buffer unit writing data-items from the stream in circular fashion into the buffer memory (the circular buffer area is an N element circular buffer, column 4, lines 10-14);

A producing process interface of the circular buffer unit (External input register, Fig. 6), arranged to use a grain size selection and an auxiliary buffer region selection particular for the data producing process (in order to deal with a wrap around condition a copy of the circular buffer is provided after the circular buffer area in memory, column 1, lines 60-64), the producing process interface being arranged to process a command for making memory available to the data producing process for writing a produced grain (Steps 121 and 122 in Fig. 8), the producing process interface being arranged to respond to the command by testing whether addresses of data within the grain for which memory has to be made available wrap around in the circular buffer memory (Step 123 in Fig. 8);

To return an indication to the producing process to write the grain to the buffer memory when the addresses do not wrap around inside the grain, or an indication to write to auxiliary memory region, when the addresses wrap around (Steps 124 and 125 in Fig. 8).

Referring to claim 9, Nadehara discloses, a machine implemented method of generating a machine implementation of a signal processing task (data is read out of data memory 4, column 4, lines 23-26), wherein the signal processing task comprises concurrently executing processes between which a data stream is communicated via a circular buffer memory (circular buffer controller in Fig. 6), the method comprising:

Providing an application program interface that includes a function to be called by a data consuming one of the processes to gain access to a grain of data stored in the buffer memory (data is read out of data memory 4, column 4, lines 23-26)

The application program interface providing for selectable definition of a size of the grain and an auxiliary memory region for the data consuming one of the processes, the function being arranged to test whether addresses of the grain to which access has to be gained wrap around in the buffer memory (Step 109, Fig. 7),

to copy the grain from the buffer memory to the auxiliary memory region when the addresses wrap around in the grain, so that the wrap around is eliminated in the copied grain, and to return as a result of the call an indication to the consuming one of the processes to read data from the grain from the buffer memory, when the addresses do not wrap around inside the grain, or an indication to read from the auxiliary memory region, when the addresses wrap around in the grain (The value of the block length register is added to the index register to move the operation through the circular buffer and if the value of the resulting value of the index is greater than the element number register, the value of the element number is subtracted from the index and the operation

occurs with the values in the wrap around portion of memory otherwise the operations are carried out on the data in the range of the circular buffer area, Figs. 7 and 9);

Receiving a specification of the signal processing task; identifying a call to said function in the specification (program memory 17 stores software to control the operation of the system, column 3-4, lines 67 and 1-2);

Implementing the call using the function from the application program interface (the instruction execution controller controls operations by referencing the program memory and comparators, column 4, lines 1-5).

As per claim 10, Nadehara discloses, a machine implemented method according to Claim 9, wherein the application program interface hides a distribution of processes over processing elements from the specification of the processing task, the implementation of the function being selected according to the distribution (the instruction execution controller 18, controls reading from the circular buffer by referencing the program memory and data from comparators, column 4, lines 1-5).

Referring to claim 12, corresponding limitations as presented in claim 1 are recited. Therefore the rejection of claim 1 applies to claim 12.

Referring to claim 13, corresponding limitations as presented in claim 8 are recited. Therefore the rejection of claim 8 applies to claim 13.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadehara US Patent No. 5,535,412 (hereinafter Nadehara) as applied to claims 1 above, and further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As per claim 4, Nadehara does not appear to explicitly disclose, the data producing process and the data consuming process are arranged to use a first and second grain size for sending data to and receiving data from the circular buffer unit respectively, the first and second grain size differing from one another.

However, the Applicant has admitted this as solved in the prior art (AAPA specification page 1, lines 25-30).

The suggestion/motivation would have been that it would be clear to one of ordinary skill that there are many applications where the output portions of a system may be fixed to a certain size, yet data may be received in a different size.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nadehara US Patent No. 5,535,412 (hereinafter Nadehara) as applied to claim 10 above, further in view of Sample et al. US Patent No. 5,477,475 (hereinafter Sample)

As per claim 11, it is noted that Nadehara does not appear to explicitly disclose, generating integrated circuit manufacturing control information for implementing the machine implementation, and manufacturing an integrated circuit under control of the integrated circuit manufacturing control information.

However, Sample discloses, generating integrated circuit manufacturing control information for implementing the machine implementation, and manufacturing an integrated circuit under control of the integrated circuit manufacturing control information (a system for integrated design where a hardware prototype is generated by a user's schematics and the prototype is electrically reconfigurable and maybe updated without changing the wiring, column 2, lines 13-20).

At the time of the invention, it would have been obvious to one of ordinary skill in the art having the teachings of Nadehara and Sample before him or her to implement the system of Nadehara on a programmable device as in Sample.

The suggestion/motivation for doing so would have been that building the system of Nadehara on an FPGA is a low cost option that would allow for updating and testing of multiple embodiments without building many prototypes. FPGA's maybe programmed to build a circuit and then reset to the build another without significant delay.

Therefore it would have been obvious to combine Sample with Nadehara to obtain the invention as specified in the instant claims

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shimizu et al. US Patent No. 5,765,187 patented on 6/9/1998 discloses a control system for a ring buffer that prevents overwriting and overrunning situations.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TUSHAR S. SHAH whose telephone number is (571)270-1970. The examiner can normally be reached on Mon-Fri 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. S. S./
Examiner, Art Unit 2184

/Manorama Padmanabhan/
For Henry Tsai
Supervisory Patent Examiner, Art Unit 2184